IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Todd Michael Burdine	:	Date: January 26, 2007
Serial No.:	10/767,046	:	IBM Corporation
Group Art Unit:	2138	:	Intellectual Property Law
Examiner:	Phung M. Chung	:	Dept. 917, Bldg. 006-1
Filed:	January 29, 2004	:	3605 Highway 52 North
Patent No.:	7,107,502 B2	:	Rochester, MN 55901-7829

Title: DIAGNOSTIC METHOD FOR DETECTION OF MULTIPLE DEFECTS IN A LEVEL SENSITIVE SCAN DESIGN (LSSD)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

PETITION FOR CERTIFICATE OF CORRECTION

In the matter of Patent Number 7,107,502 B2 issued on September 12, 2006, a careful check of the same against the file of the attorney shows errors in the patent chargeable to the Official Printer, as shown on the attached Certificate of Correction.

It is requested that the attached Certificate of Correction be certified and issued to International Business Machines Corporation, Rochester, Minnesota 55901.

Respectfully submitted,

By /james r nock/
James R. Nock
Registration No.: 42,937

Telephone: (507) 253-4661
Fax No.: (507) 253-2382

Docket No.: ROC920030281US1
Serial No.: 10/767,046

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : US 7,107,502 B2

DATED : September 12, 2006

INVENTOR(S) : Todd Michael Burdine

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Page 1, Col. 1, Line (57), should read as follows:

ABSTRACT

Methods of testing scan chains in integrated circuits are provided. One method may include steps of placing the scan chain circuit into an operating region, loading a scan test pattern into the scan chain, placing the scan chain circuit into a failing region, applying a shift clock pulse to the L2 (slave) latch, placing the scan chain circuit into an operating region, and unloading the scan chain. An additional step may be added to analyze the resulting data. Another method may include the steps of, placing the scan chain circuit into an operating region, loading a scan test pattern into the scan chain circuit, placing the scan chain circuit into a failing region, applying a scan clock pulse to the L1 (master) latch, placing the scan chain circuit into an operating region, applying a shift clock pulse to the L2 latch, and unloading the scan chain. An additional step may be added to analyze the resulting data.

22 Claims, 10 Drawing Sheets

MAILING ADDRESS OF SENDER:
James R. Nock (Reg. No. 42,937)
IBM Corporation -- Department 917
3605 Highway 52 North
Rochester, MN 55901-7829

PATENT NO. 7,107,502 B2

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